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LINK BETWEEN A CENTRAL SYSTEM AND A SATELLITE SYSTEM FOR EXECUTING OPERATIONS OF THE CENTRAL SYSTEM

[0001] The field of the invention is that of computer systems and more particularly concerns a central system from which one wishes to remote part of the execution of certain operations to a satellite system.

[0002] Remoting an execution is advantageous for example when the central system is a proprietary system. The operations of the proprietary system benefit from increased computing power and a high level of security and reliability. A satellite system from the so-called open world makes it possible to use standard hardware and software on the market.

[0003] When a task is performed entirely in a single system, the execution of the operations is fast since it runs in command control mode in devices that react in slave mode. When the execution of a task is distributed among several different systems, the prior art normally proposes having the systems communicate by means of messages. There are known architectures of the client-server type. In assigning the client function to the central system and the server function to the satellite system, the central system will establish a connection with the satellite system and send a request message to the satellite system, which will return a response message. However, the fact that the messages pass through numerous communication layers does not result in comparable performance in terms of speed relative to operations executed entirely in the same system.

[0004] To eliminate the aforementioned drawbacks of the prior art, the subject of the invention is a protocol between a central system and a satellite system for having an operation of the central system executed by the satellite system. The protocol includes:

- a first step in which the satellite system sends a read command to the central system, identified by a first logical unit number;
- a second step in which the central system responds to said read command by sending at least one data block containing said operation;
- a third step concomitant with the second step, in which the satellite system receives said data block in order to process the operation it contains.

[0005] Other advantages and details of the invention will emerge from the preferred exemplary embodiment described below in reference to the figures, in which:

Fig. 1 presents a central system, a satellite system and peripheral systems;

[illegible]

Fig. 2 present

Fig. 3 present

Fig. 4 present
Fig. 5 present
Fig. 6 present

Fig. 5 present

[0006] Referring to Fig. 1, a central system 1 generally includes one or more processors 6 that access programs and data addressed in a random access memory 7 via a bus 8. In order to be able to process data outside the direct physical address space of the memory 7, the central system 1 performs operations for accessing peripheral subsystems 2, 3, 4, 5 comprising, for example, mass storage units such as disks and magnetic tapes.

[0007] Each peripheral subsystem 2, 3, 4, 5 is identified by a logical unit number LUN. In the central system 1, a control card 9 is connected to the bus 8 in order to send read and write commands and data corresponding to the write commands to the peripheral subsystems, and to receive data that comes from the peripheral subsystems in response to the read commands.

[0008] In order to perform an operation for accessing a peripheral subsystem, the central system 1 sends an interrupt to the control card 9. Upon receiving an interrupt, the control card 9 reads in memory 7 parameters that qualify the access operation, such as the type of operation, the logical unit number that identifies the peripheral subsystem to which the operation applies, and the addresses of the memory 7 reserved for the data of the operation.

[0009] If the operation is a write operation, the control card 9 generates a write command sent to the identified peripheral subsystem, followed by the data of the operation, which is read in memory 7. Upon receiving a return status of the peripheral subsystem indicating that the write command has been correctly executed, the control card 9 generates a signal in memory 7 to inform the central system 1 that the write operation is finished.

[0010] If the operation is a read operation, the control card 9 generates a read command sent to the identified peripheral subsystem. Upon receiving the read data returned by the peripheral subsystem, the control card 9 writes the data received into memory 7 and generates a signal to inform the central system 1 that the read operation is finished.

[0018] The defined block types are the following:

- data block transmitted from the central system to the satellite system;
- data block transmitted from the satellite system to the central system;
- terminal status block;
- special status block;
- service block transmitted from the central system to the satellite system;
- service block transmitted from the satellite system to the central system;

[0019] Referring to Fig. 3, a state diagram of the satellite system 30, and to Fig. 4, a state diagram of the central system 1, each of them describes steps that may be used to implement an exchange protocol in the link 17 according to the invention.

[0020] General conventions for reading these diagrams will be used in the description below. They indicate steps 31, 35, 39 such that the passage from one step to the next is symbolized by one or more arrows, wherein an arrow between two steps is interrupted by a perpendicular line that indicates a condition 32, 37, 41 for transition to a subsequent step.

[0021] The logical state of the upstream end of an arrow is identical to the logical state of a step from which it is derived or to a logical combination of the downstream states of arrows that precede it. These logical combinations are represented by single or double horizontal lines at which one or more arrows end and from which they begin again.

[0022] A single horizontal line indicates that a disjunction (OR) of logical states of one or more arrows that end at this line has the same value as a logical disjunction of one or more arrows that start from this line.

[0023] A double horizontal line indicates that a conjunction (AND) of logical states of one or more arrows that end at this line has the same value as a logical conjunction of one or more arrows that start from this line.

[0024] In the absence of any perpendicular line that interrupts an arrow to indicate a transition, a low or high logical state of the downstream arrow is identical to an upstream logical state of the arrow.

[0025] In the presence of a perpendicular line that interrupts an arrow to indicate a transition, the downstream logical state of the arrow is equal to a logical conjunction of the upstream logical state of the arrow and the logical state of the transition indicated. A switch from the low logical state to the high logical state of the downstream end of an

[0035] The high states of the steps 34 and 35 with the high state of the transition 37 activate a step 39 by setting it to the high state and deactivate the steps 34 and 35 by setting them to the low state. Step 39 is the step for the reception of the blocks by the coupler 21. The last block of the frame coming from the logical unit with the number LUN01 sets a transition 41 to the high state.

[0036] The high states of the step 39 and the transition 41 reactivate the steps 34 and 35 by setting them to the high state and deactivate the step 39 by setting it to the low state.

[0037] The simultaneous activation of the steps 33 and 35 at the start makes it possible to optimize the transfers through the link 17 by sending a second read command without having to wait for the response to the first read command. Upon reception of the last block coming from LUN00 or LUN01, the transition 40, or respectively 41, reactivates the steps 33 and 34, or respectively 34 and 35. The possible states of the link 17 for the satellite system 30 are therefore:

- steps 33, 34 and 35 active, waiting for responses to two read commands;
- steps 33 and 39 active, waiting for a response to the read command in LUN00 and receiving a response in LUN01;
- steps 35 and 38 active, waiting for a response to the read command in LUN01 and receiving a response in LUN00;

[0038] Applying the conventions explained above to Fig. 4, the central system 1, initially in the high logical state in a reference step 42, is started by setting an initialization transition 43 to the high state. This has the effect of deactivating the step 42 by setting it to the low logical state and activating the steps 44 and 45 by setting them to the high logical state.

[0039] Step 45 sets the control card 9 in a wait state for a command via the link 17, thus determining a slave operating mode in the link 17.

[0040] Step 44 consists of forming a frame that will be transmitted to the satellite system 30 in response to a read command through the coupler 21. When the central system 1 activates an operation for accessing a peripheral subsystem 2, 3, 4, 5, the processor 6 sends the control card 9, via the bus 8, a load command for a read access or a store command for a write access. Upon reception of a load or store command, the control card 9 generates one or more blocks in the model of the one presented in Fig. 2.

1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31. 32. 33. 34. 35. 36. 37. 38. 39. 40. 41. 42. 43. 44. 45. 46. 47. 48. 49. 50. 51. 52. 53. 54. 55. 56. 57. 58. 59. 60. 61. 62. 63. 64. 65. 66. 67. 68. 69. 70. 71. 72. 73. 74. 75. 76. 77. 78. 79. 80. 81. 82. 83. 84. 85. 86. 87. 88. 89. 90. 91. 92. 93. 94. 95. 96. 97. 98. 99. 100. 101. 102. 103. 104. 105. 106. 107. 108. 109. 110. 111. 112. 113. 114. 115. 116. 117. 118. 119. 120. 121. 122. 123. 124. 125. 126. 127. 128. 129. 130. 131. 132. 133. 134. 135. 136. 137. 138. 139. 140. 141. 142. 143. 144. 145. 146. 147. 148. 149. 150. 151. 152. 153. 154. 155. 156. 157. 158. 159. 160. 161. 162. 163. 164. 165. 166. 167. 168. 169. 170. 171. 172. 173. 174. 175. 176. 177. 178. 179. 180. 181. 182. 183. 184. 185. 186. 187. 188. 189. 190. 191. 192. 193. 194. 195. 196. 197. 198. 199. 200. 201. 202. 203. 204. 205. 206. 207. 208. 209. 210. 211. 212. 213. 214. 215. 216. 217. 218. 219. 220. 221. 222. 223. 224. 225. 226. 227. 228. 229. 230. 231. 232. 233. 234. 235. 236. 237. 238. 239. 240. 241. 242. 243. 244. 245. 246. 247. 248. 249. 250. 251. 252. 253. 254. 255. 256. 257. 258. 259. 260. 261. 262. 263. 264. 265. 266. 267. 268. 269. 270. 271. 272. 273. 274. 275. 276. 277. 278. 279. 280. 281. 282. 283. 284. 285. 286. 287. 288. 289. 290. 291. 292. 293. 294. 295. 296. 297. 298. 299. 300. 301. 302. 303. 304. 305. 306. 307. 308. 309. 310. 311. 312. 313. 314. 315. 316. 317. 318. 319. 320. 321. 322. 323. 324. 325. 326. 327. 328. 329. 330. 331. 332. 333. 334. 335. 336. 337. 338. 339. 340. 341. 342. 343. 344. 345. 346. 347. 348. 349. 350. 351. 352. 353. 354. 355. 356. 357. 358. 359. 360. 361. 362. 363. 364. 365. 366. 367. 368. 369. 370. 371. 372. 373. 374. 375. 376. 377. 378. 379. 380. 381. 382. 383. 384. 385. 386. 387. 388. 389. 390. 391. 392. 393. 394. 395. 396. 397. 398. 399. 400. 401. 402. 403. 404. 405. 406. 407. 408. 409. 410. 411. 412. 413. 414. 415. 416. 417. 418. 419. 420. 421. 422. 423. 424. 425. 426. 427. 428. 429. 430. 431. 432. 433. 434. 435. 436. 437. 438. 439. 440. 441. 442. 443. 444. 445. 446. 447. 448. 449. 450. 451. 452. 453. 454. 455. 456. 457. 458. 459. 460. 461. 462. 463. 464. 465. 466. 467. 468. 469. 470. 471. 472. 473. 474. 475. 476. 477. 478. 479. 480. 481. 482. 483. 484. 485. 486. 487. 488. 489. 490. 491. 492. 493. 494. 495. 496. 497. 498. 499. 500. 501. 502. 503. 504. 505. 506. 507. 508. 509. 510. 511. 512. 513. 514. 515. 516. 517. 518. 519. 520. 521. 522. 523. 524. 525. 526. 527. 528. 529. 530. 531. 532. 533. 534. 535. 536. 537. 538. 539. 540. 541. 542. 543. 544. 545. 546. 547. 548. 549. 550. 551. 552. 553. 554. 555. 556. 557. 558. 559. 560. 561. 562. 563. 564. 565. 566. 567. 568. 569. 570. 571. 572. 573. 574. 575. 576. 577. 578. 579. 580. 581. 582. 583. 584. 585. 586. 587. 588. 589. 590. 591. 592. 593. 594. 595. 596. 597. 598. 599. 600. 601. 602. 603. 604. 605. 606. 607. 608. 609. 610. 611. 612. 613. 614. 615. 616. 617. 618. 619. 620. 621. 622. 623. 624. 625. 626. 627. 628. 629. 630. 631. 632. 633. 634. 635. 636. 637. 638. 639. 640. 641. 642. 643. 644. 645. 646. 647. 648. 649. 650. 651. 652. 653. 654. 655. 656. 657. 658. 659. 660. 661. 662. 663. 664. 665. 666. 667. 668. 669. 670. 671. 672. 673. 674. 675. 676. 677. 678. 679. 680. 681. 682. 683. 684. 685. 686. 687. 688. 689. 690. 691. 692. 693. 694. 695. 696. 697. 698. 699. 700. 701. 702. 703. 704. 705. 706. 707. 708. 709. 710. 711. 712. 713. 714. 715. 716. 717. 718. 719. 720. 721. 722. 723. 724. 725. 726. 727. 728. 729. 730. 731. 732. 733. 734. 735. 736. 737. 738. 739. 740. 741. 742. 743. 744. 745. 746. 747. 748. 749. 750. 751. 752. 753. 754. 755. 756. 757. 758. 759. 760. 761. 762. 763. 764. 765. 766. 767. 768. 769. 770. 771. 772. 773. 774. 775. 776. 777. 778. 779. 780. 781. 782. 783. 784. 785. 786. 787. 788. 789. 790. 791. 792. 793. 794. 795. 796. 797. 798. 799. 800. 801. 802. 803. 804. 805. 806. 807. 808. 809. 810. 811. 812. 813. 814. 815. 816. 817. 818. 819. 820. 821. 822. 823. 824. 825. 826. 827. 828. 829. 830. 831. 832. 833. 834. 835. 836. 837. 838. 839. 840.

[0043] When the access operation involves a store command, the control card 9 enters into the field 19 of a first block control data for specifying the store instructions with the start and end addresses of the data to be stored in the peripheral subsystem in question. The control card 9 removes one bit from the field 13 of the first block and from the field 13 of each block that precedes a subsequent block, then increments the field 16 of the next block. The bit of the field 13 is lowered for the last block of the access operation. This makes it possible to enter into the field 19 of the subsequent blocks the data to be stored in the peripheral subsystem involved in the access operation.

[0045] The blocks generated by the control card 9 are placed in a state for waiting to be transmitted through the link 17.

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in a frame whose length is compatible with the flow control, the blocks of the same type, and for data blocks, those of the same access operation.

[0047] A transition 47 is in the high state soon as a frame is available. The transition 47 resets the step 44 to the low state and sets a step 49 to the high state. Step 49 presents the previously created frame to the logical unit LUN00.

[0048] A transition 51 is in the high state if the control card 9 has received a read command through the link 17 for the logical unit LUN00. The conjunction of the high states of the steps 45, 49 and the high state of the transition 51 activates a step 53 by setting it to the high state and resets the steps 45 and 49 to the low state.

[0049] In step 53, the blocks of the frame presented in the logical unit LUN00 are sent through the link 17 to the coupler 21.

[0050] The last block of the frame sent sets a transition 55 to the high state. The conjunction of the high states of the step 53 and the transition 55 resets the step 53 to the low state and reactivates the steps 44 and 45 by setting them to the high state. This makes it possible to send other blocks, for example for other access operations or for the continuation of the same access operation.

[0051] In addition to the transition 32 and the step 35 for taking advantage of the transfer capacities of the link 17, the conjunction of the high logical states of the reference step 42 and the initialization step 43 also activates a step 46 by setting it to the high logical state.

[0052] As with the step 44, setting the step 46 to the high state triggers two actions. A first action scans the waiting blocks. A second action removes a timeout in the case where no block is waiting to be transmitted. If no block is waiting at the end of the timeout, the control card 9 creates an empty block, i.e. a block that is constituted by a simple header without a field 19 and that leaves its type empty in the field 10. This makes it possible to transmit a response to the read order coming from the coupler 21, so as not to detect any false errors in the link 17 in the absence of blocks to be transmitted. The control card 9 then collects, in a frame whose length is compatible with the flow control, the blocks of the same type, and for data blocks, those of the same access operation.

[0053] A transition 48 is in the high state soon as a frame is available. The transition 48 resets the step 46 to the low state and sets a step 50 to the high state. Step 50 presents the previously created frame to the logical unit LUN01.

[0054] A transition 52 is in the high state if the control card 9 has received a read command through the link 17 for the logical unit LUN01. The conjunction of the high states of the steps 45, 50 and the high state of the transition 52 activates a step 54 by setting it to the high state and resets the steps 45 and 50 to the low state.

[0055] In step 54, the blocks of the frame presented in the logical unit LUN01 are sent through the link 17 to the coupler 21.

[0056] The last block of the frame sent sets a transition 56 to the high state. The conjunction of the high states of the step 54 and the transition 56 resets the step 53 to the low state and reactivates the steps 46 and 45 by setting them to the high state. This makes it possible to send other blocks, for example for other access operations or for the continuation of the same access operation.

[0057] The possible states of the link 17 for the central system 1 are therefore:

- steps 44, 45 and 46 active, waiting for frames to transmit;
- steps 44, 45 and 50 active waiting for a frame for LUN00 and waiting for a read operation for LUN01;
- steps 49, 45 and 46 active, waiting for a read operation for LUN00 and waiting for a frame for LUN01;
- steps 49, 45 and 50 active, waiting for a read operation for LUN00 and for LUN01;
- steps 53 and 46 or 50 active, waiting for the end of a transmission from LUN00;
- steps 54 and 44 or 49 active, waiting for the end of a transmission from LUN01.

[0058] Referring to Fig. 5, the frames received in the coupler 21 in steps 38 and 39 are processed by the satellite system 30 in the following way:

[0059] Upon receiving a block in accordance with the protocol explained in reference to the preceding figures, the satellite system 30 stores this block in an incoming buffer 72, 73, 74 corresponding to the logical channel contained in the field 11;

[0060] Upon receiving the last block from the same logical channel, the satellite system 30 sends the content of the buffer 72, 73, 74 to the coupler 22, 23, 24, 25 corresponding to the physical channel contained in the field 15, adapting the commands to this coupler.

[0061] The coupler 22, 23, 24 25 returns a response stored in an outgoing buffer 75.

[0062] The satellite system 30 transmits the content of the buffer 75 to the coupler 29 in the sequence of the protocol explained in reference to the following figures.

[0063] For example, in step 38, the coupler 21 receives a frame comprising the blocks 57, 58. The field 11 of these blocks identifies a logical channel corresponding to the buffer 72 contained in memory 27. The satellite system 30 stores the blocks of the frame in the buffer 72 via the bus 28. The field 13 of the block 58 indicates that there are other blocks to follow for the same logical channel.

[0064] In step 39, the coupler 21 receives a frame comprising a block 59. The field 11 of this block identifies a logical channel corresponding to the buffer 72 contained in memory 27. The satellite system 30 stores the block of the frame in the buffer 72 via the bus 28. The field 13 of the block 59 indicates that there are other blocks to follow for the same logical channel.

[0065] In step 39, the coupler 21 receives a frame comprising a block 60. The field 11 of this block identifies a logical channel corresponding to the buffer 73 contained in memory 27. The satellite system 30 stores the block of the frame in the buffer 73 via the bus 28. The field 13 of the block 60 indicates that it is the last block from this logical channel.

[0066] The field 19 of the block 60 contains load commands. The satellite system 30 creates a control block 60' from the field 19. The field 15 of the block 60 identifies a physical channel corresponding to the coupler 22. The satellite system 30 transmits the block 60' to the coupler 22 via the bus 28.

[0067] In step 38, the coupler 21 receives a frame comprising a block 61. The field 11 of this block identifies a logical channel corresponding to the buffer 72 contained in memory 27. The satellite system 30 stores the block of the frame in the buffer 72 via the bus 28. The field 13 of the block 61 indicates that it precedes another block from the same logical channel.

[0068] In step 39, the coupler 21 receives a frame comprising blocks 62, 63. The field 11 of these blocks identifies a logical channel corresponding to the buffer 74 contained in memory 27. The satellite system 30 stores the block of the frame in the buffer 74 via the bus 28. The field 13 of the block 63 indicates that there is no other block to follow for the same logical channel.

[0071] In step 39, the coupler 21 receives a frame comprising a block 65. The field 11 of this block identifies a logical channel corresponding to the buffer 72 contained in memory 27. The satellite system 30 stores the block of the frame in the buffer 72 via the bus 28. The field 13 of the block 65 indicates that there is no other block to follow for the same logical channel.

[0073] The coupler 22 executes, in the peripheral subsystem 2, the load command specified by the block 60'. The peripheral subsystem then returns data blocks 66', 67', 68' and a status block 69' to the coupler 22. The satellite system 30 then places each block 66', 67', 68', 69' in the field 19 of a block 66, 67, 68, 69 in accordance with the protocol described previously. In particular, the field 10 indicates that the block type is a data block transmitted from the satellite system to the central system, the field 11 identifies the same logical channel as the field 11 of the block 60. The field 13 of each of the blocks 66, 67, 68 indicates that the block precedes another block from the same logical channel. The field 13 of the block 69 indicates that the block does not precede any other block from the same logical channel. The satellite system 30 stores the blocks 66, 67, 68, 69 in the buffer 75 via the bus 28.

[0074] The coupler 24 executes, in the peripheral subsystem 4, the store command specified by the block 62'. The peripheral subsystem then returns a status block 70' to the coupler 24. The satellite system 30 then places the block 70' in the field 19 of a block 70 in accordance with the protocol described previously. In particular, the field 10 indicates that the block type is a data block transmitted from the satellite system to the central system, and the field 11 identifies the same logical channel as the field 11 of the block 62. The field 13 of each of the block 70 indicates that the block does not precede any other block from the same logical channel. The satellite system 30 stores the block 70 in the buffer 75 via the bus 28.

[0075] The coupler 22 executes, in the peripheral subsystem 2, the store command specified by the block 57'. The peripheral subsystem then returns a status block 71' to the coupler 22. The satellite system 30 then places the block 71' in the field 19 of a block 71 in accordance with the protocol described previously. In particular, the field 10 indicates that the block type is a data block transmitted from the satellite system to the central system, and the field 11 identifies the same logical channel as the field 11 of the block 57. The field 13 of the block 71 indicates that the block does not precede any other block from the same logical channel. The satellite system 30 stores the block 71 in the buffer 75 via the bus 28.

[0076] The frames contained in the buffer 75 are sent through the link 20 by means of the coupler 29, in accordance with the state diagram of Fig. 6.

[0077] Applying the conventions explained above to Fig. 6, the satellite system 30, initially in the high logical state in a reference step 76, is started by setting an initialization transition 77 to the high state. This has the effect of deactivating the step 76 by setting it to the low logical state and activating the steps 78 and 79 by setting them to the high logical state.

[0078] Step 79 declares the link U available for a transfer of blocks from the card of the coupler 29 to the control card 9.

[0079] Step 78 reads the outgoing buffer 75 in order to detect whether a frame is ready to be transmitted to a logical unit number LUN10. Thus, the satellite system 30 sees the central system 1 as a storage unit, such as for example a magnetic tape, with the logical unit number LUN10.

[0080] The detection of a frame in the buffer 75 that the step 78 decides to send to the logical unit with the number LUN10, sets a transition 81 to the high state.

[0083] In a way that improves the performance of the link 20, setting the transition 77 to the high state has the additional effect of setting a step 80 to the high state.

[0085] The detection of a frame in the buffer 75 that the step 80 decides to send to the logical unit with the number LUN11, sets a transition 82 to the high state.

[0087] The high states of the step 84 and the transition 86 reactivate the steps 80 and 79 by setting them to the high state and deactivate the step 84 by setting it to the low state.

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- steps 78, 79 and 80 active, waiting for frames in the buffer 75;
- steps 78 and 84 active, waiting for the end of a write operation in LUN11;
- steps 80 and 83 active, waiting for the end of a write operation in LUN10;

[0089] Returning to the example of Fig. 4, the reading of the buffer 75 in step 78 detects a frame constituted by the data block 66. A write command LUN10 and the block 66 are sent in step 83.

[0090] The reading of the buffer 75 in step 80 detects a frame constituted by the data block 67. After the transmission of the block 66, the steps 79 and 78 are reactivated. A write command LUN11 and the block 67 are sent in step 84. The reading of the buffer 75 in step 78 detects a frame constituted by data blocks 68 and 69. After the transmission of the block 67, the steps 79 and 80 are reactivated. A write command LUN10 and the blocks 68 and 69 are sent in step 83. The reading of the buffer 75 in step 80 detects a frame constituted by the data block 70. After the transmission of the blocks 68 and 69, the steps 79 and 78 are reactivated. A write command LUN11 and the block 70 are sent in step 84.

[0091] When the control card 9 has received the blocks 66 through 69 wherein the field 11 indicates the same logical channel as the field 11 of the block 60, it provides through the bus 8 a response to the load command it had sent in the field 19 of the block 60. The response is constituted by the content of the fields 19 of the blocks 66 through 68, loaded into memory 7. The control card 9 also sends through the bus 8 the content of the field 19 of the block 69 in order to indicate to the central system 1 that the load operation is finished.

[0092] When the control card 9 has received the block 70 wherein the field 11 indicates the same logical channel as the field 11 of the block 62, it provides through the bus 8 a response to the store command it had sent in the field 19 of the block 62. The response is constituted by the content of the field 19 of the block 70, so as to indicate to the central system 1 that the store operation is finished.

[0093] One skilled in the art can easily understand from the preceding description that the operations of the central system are not limited to operations for accessing storage units. The teaching of the invention can advantageously be extended to communication operations in networks like the Internet, for example by replacing the coupler 25 with a network access card.